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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/496,374	02/02/2000	Masami Kidono	OOCL-11 (11P024627)	6123

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EXAMINER	
PIZIALI, JEFFREY J	

ART UNIT	PAPER NUMBER
2673	21

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/496,374	KIDONO ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3 June 2004 (Paper No. 21)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 12-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3 June 2004 (Paper No. 21) has been entered.

Drawings

2. The drawings were received on 8 September 2003 (Paper No. 15). These drawings are acceptable.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-9 and 12-23 are rejected under 35 U.S.C. 102(a) as being anticipated by the current application's own admitted prior art.

Regarding claim 1, the background of the current invention discloses a solid-state imaging device comprising: a pixel unit [Fig. 7, 1] constituted by a two-dimensional array of

pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time; a vertical transfer unit [Fig. 7, 2] for vertically transferring charge from the pixels in the pixel unit; a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit; shift gates [Fig. 7, 3] each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes [Fig. 7, 4A -- horizontal lines] for controlling the shift gates; and a plurality of lead lines [Fig. 7, 4A -- vertical lines] for connecting the gate electrodes to an external circuit and a plurality of connection terminals [Fig. 7, 6] for connecting the gate electrodes to the external circuit; the gate electrodes making up N [where N = 6, for instance] of gate electrode groups in which the lines belonging to each coset of modulo 6 within successive pixel rows are connected to common lead lines, 6 being a predetermined natural number between 4 and one half the number of pixels [where the number of pixels = 12, for instance] in a column, and also being the minimum number corresponding to the periodic unit about connections from the gate electrodes to the connection terminals within the successive pixel rows, the gate electrodes having common connection terminals to reduce the number (i.e. from 3 to 2, for instance) of the connection terminals to less than 12 (see Page 2, Line 15 - Page 5, Line 6).

Regarding claim 2, this claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, the background of the current invention discloses gate electrodes/gate control lines [Fig. 7, 4A] connected to gate electrode groups in which horizontal lines belonging to each coset of modulo 6 [where N=6, for instance] within successive pixel rows are connected commonly, being combined with each other so as to reduce the number (i.e. from

3 to 2, for instance) of the connection terminals to less than 6 (see Page 2, Line 15 - Page 5, Line 6).

Regarding claim 3, this claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, the background of the current invention discloses the gate electrodes being provided in a predetermined number 6 [where N = 6, for instance] of gate electrode groups such that the horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo 6, 6 being a predetermined natural number between 4 and one half the number of pixels [where the number of pixels = 12, for instance] in a column, and also being the minimum number corresponding to the periodic unit about connections from the gate electrodes to the connection terminals within the successive pixel rows, some of the gate electrode groups being commonly connected so that the connection electrodes are less in number (i.e. from 3 to 2, for instance) than 6 (see Page 2, Line 15 - Page 5, Line 6).

Regarding claim 4, this claim is rejected under the reasoning applied in the above rejection of claim 1; furthermore, the background of the current invention discloses the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving (see Fig. 7; Page 4, Line 8 - Page 5, Line 6).

Regarding claim 5, this claim is rejected under the reasoning applied in the above rejection of claims 1, 2 and 4.

Regarding claim 6, this claim is rejected under the reasoning applied in the above rejection of claims 1, 3 and 4.

Regarding claims 7-9, the background of the current invention discloses gate electrode groups controlled in each of all the predetermined read-out modes are set such as to provide a minimum number of connection terminals for connecting the gate electrodes to an external circuit (see Fig. 7; Page 4, Line 8 - Page 5, Line 6; where 2 connection terminals is the minimum in this modulo 6 example).

Regarding claims 12-17, the background of the current invention discloses at least two horizontal lines belonging to the same pixel group but to different gate electrode groups are connected to a common connection terminal (see Fig. 7; Page 2, Line 15 - Page 5, Line 6).

Regarding claims 18-23, the background of the current invention discloses only two connection terminals connected to the vertical transfer unit are not connected to any of the gate electrodes (see Fig. 7; Page 2, Line 15 - Page 5, Line 6).

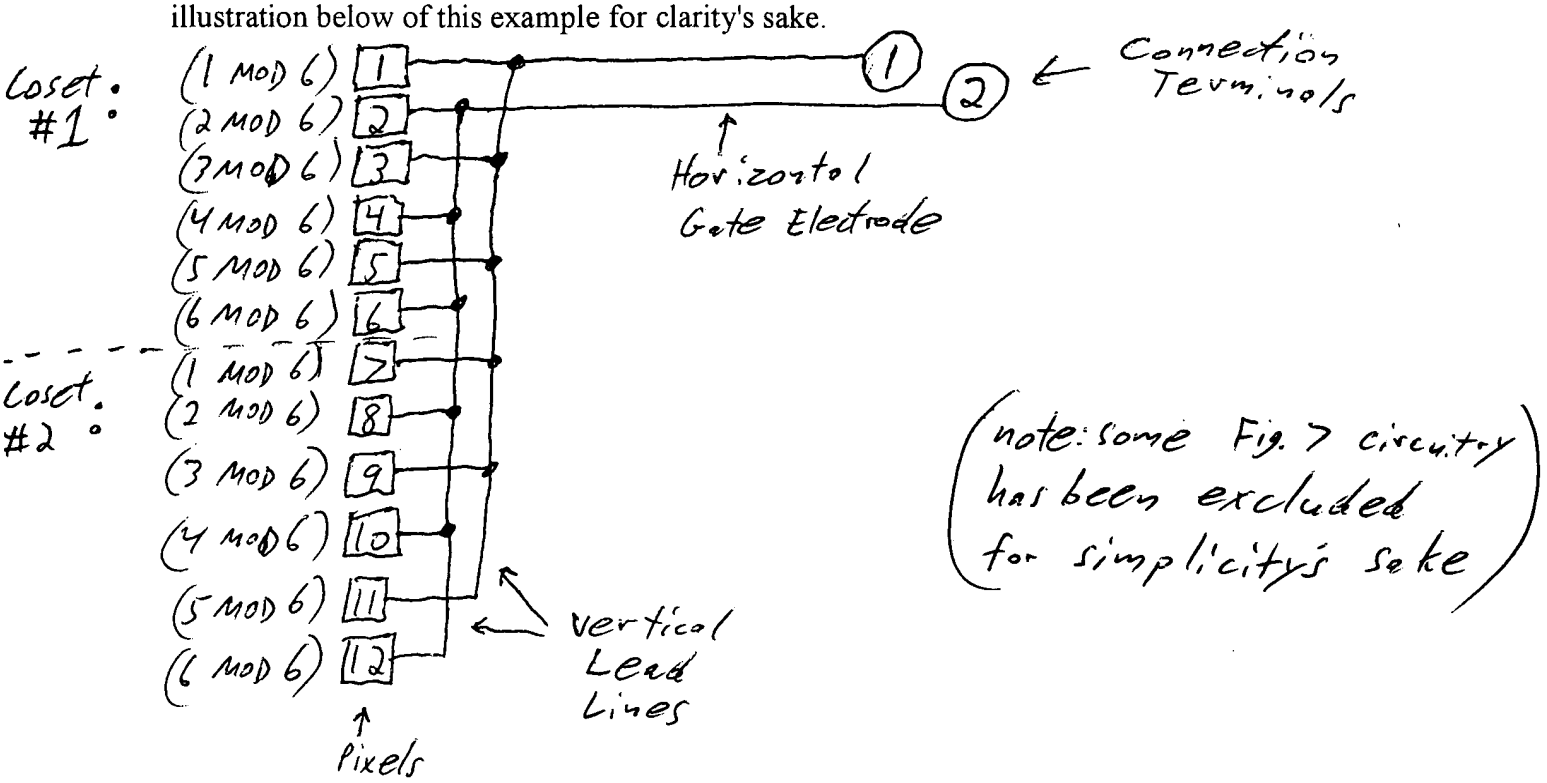
Response to Arguments

5. Applicants' arguments filed 3 June 2004 (Paper No. 21) have been fully considered but they are not persuasive. The applicants contend that the current application's own admitted prior art does not teach a plurality of lead lines for connecting the gate electrodes to an external circuit and a plurality of connection terminals for connecting the gate electrodes to the external circuit. However, the examiner respectfully disagrees. The prior art Figure 7 illustrates a plurality of lead lines [Fig. 7, 4A -- vertical lines] for connecting the gate electrodes [Fig. 7, 4A -- horizontal lines] to an external circuit and a plurality of connection terminals [Fig. 7, 6] for connecting the gate electrodes to the external circuit (see Page 2, Line 15 - Page 5, Line 6).

Additionally, the applicants contend that the current application's own admitted prior art does not teach the gate electrodes making up N of gate electrode groups in which the lines belonging to each coset of modulo N within successive pixel rows are connected to common lead lines. However, the examiner must again respectfully disagree. Although Figure 7 illustrates an imaging device with 16 connection terminals; the examiner, for reasons of brevity and conceptual simplicity, will instead rely upon an example duplicating Figure 7's pixel-to-terminal wiring design, but only comprising two connection terminals. It is noted however, the following example circuitry arrangement can be easily extrapolated to include 16 (or more) connection terminals -- increasing the modulo and complexity accordingly.

In this example, there are twelve pixels [Fig 7; 1]. Two connection terminals [Fig. 7; 6]. The gate electrodes [Fig. 7; 4A - horizontal lines] making up six (where N = 6) of gate electrode groups -- effectively dividing the twelve pixels total into two separate cosets of six pixels each. Connection terminal #1 is connected to odd-numbered pixels 1, 3, 5, 7, 9, & 11. Connection

terminal #2 is connected to even-numbered pixels 2, 4, 6, 8, 10, & 12. That is, in other words, connection terminal #1 is connected to pixels 1 MOD 6, 3 MOD 6, & 5 MOD 6; and connection terminal #2 is connected to pixels 2 MOD 6, 4 MOD 6, & 6 MOD 6 -- this remains true for the first coset of 6 pixels as well as the second coset of 6 pixels. The examiner has included a rough illustration below of this example for clarity's sake.



Following from the above example, it is clearly evidenced that current application's own admitted prior art does teach the gate electrodes making up N of gate electrode groups in which the lines belonging to each coset of modulo N within successive pixel rows are connected to common lead lines. The above example, with only ***2 connection terminals*** and ***12 pixels***, is ***modulo 6***. However, Figure 7, with ***16 connection terminals*** and ***544 pixels***, would be ***modulo 272***. By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J.P.
25 June 2004

Amare Mengistu
Primary Examiner